Amendments in the Abstract

ABSTRACT

Systems and methods for delay-fault testing field programmable gate arrays (FPGA's), applicable both for off-line manufacturing and system-level testing, as well as for on-line testing within the framework of the roving self-test area (STARs) approach are described. In one described method ~~according to the present invention~~, two or more paths under test receive a test pattern approximately simultaneously. The two paths are substantially identical and thus should propagate the signal in approximately the same amount of time. An output response analyzer receives the signal from each of the paths and determines the interval between them, and then~~.~~ ~~The output response analyzer next~~ determines whether a delay fault has occurred based at least in part on the interval. ~~In one embodiment, t~~The output response analyzer may include~~comprises~~ an oscillator and a counter. The oscillator generates an oscillating signal during the interval between when the test signal propagates through the first path ~~under test~~ and ~~when the test signal propagates through~~ the last path under test.